provision of a further negative DC feedback path connected between the output of NOT gate U4 and the control input i.e. the gate of FET Q1. To this end, a simple, single RC low pass filter (R_5,C_5) provides sufficient filtering to establish the mean output level. In this way, the NOT gate U4 is automatically 'self-biased' to the correct switching level.

IN THE CLAIMS:

Please amend claims 1-2, 6, 12-13, 27, and 30 as follows:

1. (Amended) An anti-jitter circuit for reducing time jitter in an input pulse train comprising,

an integrator charge storage means <u>for storing charge</u>,

charging means for deriving from the input pulse train at least one charge packet during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means,

discharging means for continuously discharging the integrator charge storage means,

the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage waveform, [having a mean d.c. voltage level, and]

<u>a low pass filter coupled to said integrator charge storage means for deriving a mean d.c. voltage level of said time varying voltage waveform, and</u>

means for comparing said time varying voltage waveform with said mean d.c. voltage level and deriving an output pulse train as a result of the comparison.

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2. (Amended) An anti-jitter circuit as claimed in claim 1 wherein said discharging means comprises a discharge device having a control input and said low pass filter defines [means defining] a negative feedback path between the control input and an output of the integrator charge storage means whereby to maintain said mean d.c. voltage level substantially constant.

5. (Cancelled)

6. (Amended) An anti-jitter circuit as claimed in claim 1 [5] wherein the low pass filter [negative feedback path] comprises [is formed by] the combination of a resistor and a capacitor.

12. (Twice Amended) An anti-jitter circuit as claimed in claim 8 wherein said monostable circuit is triggered whenever a discharge part of the time-varying voltage waveform crosses the mean d.c. voltage level.

13. (Twice Amended) An anti-jitter circuit as claimed in claim 1 [including frequency doubling means] comprising a first said charging means and a second said charging means for deriving charge packets respectively from the rising and falling edges of the input pulse train, said first and second charging means being effective as a frequency doubling means.

27. (Amended) An anti-jitter circuit as claimed in claim [any one of claims] 1 [to 26] wherein [the or each] said charging means is a charge pump.

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30. (Amended) An anti-jitter circuit as claimed in claim 29 wherein said low pass filter comprises the combination [combiantion] of a resistor and a capacitor.

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